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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,664	11/18/2003	Sung-Min Kim	5649-1175	5373

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D. Scott Moore, Esq.
Myers Bigel Sibley & Sajovec, P.A.
P.O. Box 37428
Raleigh, NC 27627

EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/715,664	KIM ET AL.	
	Examiner	Art Unit	
	Thomas L Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) *21-36* is/are withdrawn from consideration.

5)☒ Claim(s) *9-16* is/are allowed.

6)☒ Claim(s) *1,2,7 and 17* is/are rejected.

7)☒ Claim(s) *3-6,8 and 18-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2003 and 09 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/18/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 10/12/2004 has been entered.

Election/Restriction

2. Applicant's election without traverse of Group II, claims 1-20, in the Paper received 10/12/2004 is acknowledged.

Oath/Declaration

3. The oath/declaration filed on 11/18/2003 is acceptable.

Drawings

4. The formal drawings filed on 11/18/2003 and 03/09/2004 are acceptable.

Priority

5. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

6. The Information Disclosure Statement filed on 11/18/2003 has been considered.

Claim Objections

7. Claim 19 is objected to because of the following informalities:

There is no apparent antecedent basis for "the isolation layer," in claim 19. Applicants may have intended to make claim 19 dependent from claim 18 (where the term "isolation layer" is first introduced) but this is not presently the case.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,2,7, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by SKOTNICKI ET AL. (EP 1091417 A1).

With regard to claims 1,2, and 7 Skotnicki et al. discloses a double gate MOS transistor comprising a substrate active region 2 defined in a semiconductor substrate 1; a transistor active region 5a located over the substrate active region 2 and overlapped with the substrate active region 2; at least one semiconductor pillar 5b penetrating the transistor active region 5a and being in contact with the substrate active region 2, the at least one semiconductor pillar 5b supporting the transistor active region 5a so that the

transistor active region 5a is spaced apart from the substrate active region 2; at least one bottom gate electrode (the bottom portion of all around gate 10) substantially filling a space between the transistor active region 5a and the substrate active region 2, the at least one bottom gate electrode being insulated from the substrate active region 2, the transistor active region 5a and the semiconductor pillar 5b; and at least one top gate electrode (top portions of all around gate 10) crossing over the transistor active region 5a, and having at least one end that is in contact with a sidewall (the walls forming the upright sides of all around gate 10 as it wraps around transistor active region 5a) of the at least one bottom gate electrode, wherein the at least one top gate electrode overlaps with the bottom gate electrode, the at least one top gate electrode is insulated from the transistor active region 5a, and the at least one semiconductor pillar 5b is (comprises) a single semiconductor pillar 5b (either the left or right hand pillar 5b may be the claimed single pillar) penetrating a portion of the transistor active region 5a or includes (comprises) a first semiconductor pillar 5b and a second semiconductor pillar 5b (note that it takes both the left hand and the right hand pillars 5b to meet the claimed first and second pillars) located on both edges of the transistor active region 5a and the bottom gate electrode respectively, and the at least one bottom gate electrode is a single bottom gate electrode.

With regard to claim 17 Skotnicki et al. discloses a double gate MOS transistor comprising an isolation layer 8 formed at a portion of a semiconductor substrate 1 to define a substrate active region 2; a transistor active region 5a disposed over the

substrate active region 2 and overlapped with the substrate active region 2; a first semiconductor pillar 5b (left hand instance) and a second semiconductor pillar 5b (right hand instance) disposed at both sides of the transistor active region 5a respectively, the first and second semiconductor pillars 5b contacting the substrate active region 2; a bottom gate electrode (the bottom portion of all around gate 10) substantially filling a space between the transistor active region 5a and the substrate active region 2, the bottom gate electrode being insulated from the substrate active region 2, the transistor active region 5a, the first semiconductor pillar 5b and the second semiconductor pillar 5b; and first and second parallel top gate electrodes (top portions of all around gate 10) crossing over the transistor active region 5a, each of the first and second top gate electrodes having both ends that are in contact with sidewalls (the sidewalls being side portions of all around gate 10 seen at the front and the back – measuring right and left by the pillars 5b – of transistor active region 5a) of the bottom gate electrode, and being located between the first and second semiconductor pillars 5b to overlap with the bottom gate electrode.

Note figures 1A-1E and paragraphs 14-42 of Skotnicki et al.

Allowable Subject Matter

9. Claims 9-16 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as the double gate (note that since applicant's top gate is in contact with applicant's gate

sidewall which in turn contacts applicant's bottom gate, it would be at least as appropriate to term the invention a "GAA," or "gate-all-around") MOS transistor, having in particular a central semiconductor pillar intersecting the central portion of the transistor active region (TAR) to divide said TAR into 1st and 2nd TARs, as recited in both of claims 9 and 13. Skotnicki et al. 6,495,403, whose French language equivalent EP 1091417 A1 is cited above against claims 1,2,7, and 17, discloses many of the elements of claims 9 and 13, but Skotnicki et al. neither discloses nor suggests this particular feature.

10. Claims 3-6,8 and 18-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thomas L. Dickey
Patent Examiner
Art Unit 2826
12/04